AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Original) Apparatus for processing data, said apparatus comprising:

(i) a processing circuit operable to process data values under control of processing instructions;

(ii) a memory operable to store data values to be processed, said processing circuit being responsive to a data access instruction to access a data value stored within said memory; and

(iii) a tracing circuit operable to generate a stream of trace data identifying processing instructions executed and data values accessed by said processing circuit; wherein

(iv) a data access instruction may result in a data miss such that a data value corresponding to said data access instruction is accessed upon a processing cycle subsequent to that upon which said access would occur without said data miss; and

(v) said tracing circuit is responsive to said data miss to generate a data place holder within said stream of trace data at a position where data identifying said data value would have been placed if said data miss had not occurred and then, when said access to said data value does occur, to insert at a later point in said stream of trace data a late data value identifying said data value.

2. (Original) Apparatus as claimed in claim 1, wherein said memory comprises a cache memory and a main memory, a data miss occurring when a data value being accessed is not stored within said cache memory.

3. (Original) Apparatus as claimed in claim 1, wherein said data place holder includes a tag value and said late data value includes a matching tag value.

4. (Original) Apparatus as claimed in claim 3, wherein when a plurality of data misses result in a plurality of data place holders being generated, late data values may be generated in a different order than their corresponding data misses.

5. (Original) Apparatus as claimed in claim 1, wherein said data place holder includes data identifying how many outstanding late data values are awaited at that time.

6. (Previously Presented) Apparatus as claimed in claim 1, wherein said stream of trace data includes periodic synchronizing data, said synchronizing data including data identifying how many outstanding late data values are awaited at that time.

7. (Original) Apparatus as claimed in claim 1, wherein said tracing circuit is operable to control tracing operation in response to a trigger condition associated with one or more of said data value and a memory address associated with said data value.

8. (Original) Apparatus as claimed in claim 7, wherein said tracing circuit is responsive to an exact match signal such that a trigger condition associated with a data value for which a data miss occurs is either:

(i) not triggered until said data value is accessed and found to meet said trigger condition; or

(ii) triggered upon said data miss upon an assumption that said data value when accessed will meet said trigger condition.

9. (Original) Apparatus as claimed in claim 8, wherein said exact match signal is user configurable.

10. (Original) Apparatus as claimed in claim 8, wherein said exact match signal is set under hardware control depending upon a use of said trigger condition.

11. (Currently Amended) Apparatus as claimed in claim 8, wherein said exact match signal has different values in different parts of said tracing circuit to ~~provide both behaviors~~ simultaneously provide behaviors whereby said tracing circuit is responsive to an exact match signal such that a trigger condition associated with a data value for which a data miss occurs is either:

(i) not triggered until said data value is accessed and found to meet said trigger condition; or

(ii) triggered upon said data miss upon an assumption that said data value when accessed will meet said trigger condition.

12. (Previously Presented) A method of processing data, said method comprising the steps of:

(i) processing data values under control of processing instructions;

(ii) storing data values to be processed, a data access instruction being operable to access a stored data value; and

(iii) generating a stream of trace data identifying processing instructions executed and data values accessed; wherein

(iv) a data access instruction may result in a data miss such that a data value corresponding to said data access instruction is accessed upon a processing cycle subsequent to that upon which said access would occur without said data miss; and

(v) in response to said data miss, generating a data place holder within said stream of trace data at a position where data identifying said data value would have been placed if said data miss had not occurred and then, when said access to said data value does occur, inserting at a later point in said stream of trace a late data value identifying said data value.

13. (Previously Presented) A computer program product carrying out a computer program for controlling a data processing apparatus to analyze a stream of trace data generated in accordance with the method of claim 12.

14. (Previously Presented) Apparatus for processing data, comprising:

means for processing data values under control of processing instructions;

means for storing data values to be processed, said processing means being responsive to a data access instruction to access a data value stored within said memory means;

means for generating a stream of trace data identifying processing instructions executed and data values accessed by said processing circuit; and

means for accessing a data value corresponding to a data access instruction resulting in a data miss at a processing cycle subsequent to that at which said access would occur without said data miss;

wherein the means for generating is responsive to said data miss to generate a data place holder within said stream of trace data at a position where data identifying said data value would have been placed if said data miss had not occurred and the, when said access to said data value does occur, to insert at a later point in said stream of trace data a late data value identifying said data value.

15. (Currently Amended) Apparatus as claimed in claim ~~16~~ 14, wherein said means for storing comprises a cache memory and a main memory, a data miss occurring when a data value being accessed is not stored within said cache memory.

16. (Previously Presented) Apparatus as claimed in claim 14, wherein said data place holder includes a tag value and said late data value includes a matching tag value.

17. (Previously Presented) Apparatus as claimed in claim 14, wherein when a plurality of data misses result in a plurality of data place holders being generated, late data values may be generated in a different order than their corresponding data misses.

18. (Previously Presented) Apparatus as claimed in claim 14, wherein said data place holder includes data identifying how many outstanding late data values are awaited at that time.

19. (Previously Presented) Apparatus as claimed in claim 14, wherein said stream of trace data includes periodic synchronizing data, said synchronizing data including data identifying how may outstanding late data values are awaited at that time.

20. (Previously Presented) Apparatus as claimed in claim 14, wherein said means for generating is a tracing circuit operable to control a tracing operation in response to a trigger condition associated with one or more of said data value and a memory address associated with said data value.

21. (Previously Presented) Apparatus as claimed in claim 20, wherein said means for generating is responsive to an exact match signal such that a trigger condition associated with a data value for which a data miss occurs is either:

(i) not triggered until said data value is accessed and found to meet said trigger condition; or

(ii) triggered upon said data miss upon an assumption that said data value when accessed will meet said trigger condition.

22. (Previously Presented) Apparatus as claimed in claim 21, wherein said exact match signal is user configurable.

23. (Previously Presented) Apparatus as claimed in claim 21, wherein said exact match signal is set under hardware control depending upon a use of said trigger condition.

24. (Currently Amended) Apparatus as claimed in claim ~~14~~ 21, wherein said exact match signal has different values in different parts of said means for generating to ~~provide both behaviors~~ simultaneously provide behaviors whereby said means for generating is responsive to an exact match signal such that a trigger condition associated with a data value for which a data miss occurs is either:

(i) not triggered until said data value is accessed and found to meet said trigger condition; or

(ii) triggered upon said data miss upon an assumption that said data value when accessed will meet said trigger condition.